

UNITED STATES PATENT APPLICATION

DEVICE AND METHOD FOR CONTROLLING VOLTAGE VARIATION

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DEVICE AND METHOD FOR CONTROLLING VOLTAGE VARIATION

Field of the Invention

This invention relates to controlling voltage variations, and more particularly to using voltage variable capacitors to control voltage variations in electronic systems.

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Background of the Invention

As synchronous digital systems are operated at lower voltages, multiple voltages, and higher frequencies, and as the number of logic cells that make up the systems increase, new problems arise in supplying power to the systems. Some of the problems include decoupling multiple voltage power supplies, damping power supply grid network resonances, and decoupling noise in power supply signals operating at low voltages.

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For digital systems fabricated using mixed technologies and multiple voltages on a single substrate, the acceptable variation in the voltages are becoming more complex. For example, a system specification may define acceptable variations that are asymmetrical in the voltages. In a system requiring a 1.8 volt power supply and a 1.0 volt power supply, the 1.0 volt power supply may be required to maintain a value above 1.02 volts while the 1.8 volt supply may be permitted to rise to 2.0 volts. Digital systems having such specifications are typically decoupled by connecting a number of individual capacitive elements to each power supply voltage line near the logic cells being powered. Unfortunately, fabricating a number of separate capacitive elements for each cell and for each power supply line is very expensive in terms of space on the surface of the substrate.

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Synchronous digital systems, such as microprocessors, packaged using controlled collapse chip connection technology can have hundreds of power connection points coupled to hundreds of thousands of digital cells decoupled by hundreds of thousands of fixed capacitors. The circuit formed by the power supply, the power lines, the parasitic inductances and capacitors, the power connection points, the digital cells, and the fixed capacitors form a power connection grid network. For large transient current events that occur in synchronous digital systems, the network can experience resonant oscillations. During the development of synchronous digital systems, simulations of the logic circuits

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that comprise the system are run to identify sequences of operations that result in large transient current events capable of producing resonant oscillations. Capacitors are added to the power connection grid network to reduce the magnitude of the current events and damp out any resulting resonant oscillations. Unfortunately, simulations seldom reflect the actual operating conditions of a complex circuit, and for complex synchronous digital systems it is difficult to simulate all possible modes of operations in a way that guarantees that resonant oscillations will not occur during the operation of the system.

Synchronous digital systems implemented as integrated circuits on a semiconductor substrate periodically demand large amounts of current. This demand is supplied by fixed capacitors located on the substrate and charged to a nominal operating voltage. As long as the variation in the nominal operating voltage is less than about 10% of the operating voltage, the logical operation of the synchronous digital system is unaffected. However, the trend in the design of synchronous digital systems is to reduce the nominal operating voltage and the absolute variation in the nominal operating voltage. Unfortunately, at the same time the acceptable variation in the nominal operating voltage is decreasing, the number of switching circuits on the substrate is increasing. Increasing the number of switching circuits increases the demand for current in the switching circuits, which increases the noise in the system. One solution to this problem is to increase the number of fixed capacitors coupled to the switching circuits. Unfortunately, for complex synchronous digital systems, such as microprocessors, the fixed capacitors already occupy a large percentage of the substrate area.

For these and other reasons there is a need for the present invention.

Summary of the Invention

In some embodiments, the invention includes a noise reduction device comprising complementary metal-oxide semiconductor (CMOS) transistor. The transistor is operable as a two-terminal device in a depletion mode and has a non-linear voltage variation for charge being removed at a constant rate. The transistor is formed in an n-type substrate having an n-type drain, an n-type source, an p-type polysilicon gate, and a gate oxide layer.

Other embodiments are described and claimed below.

Brief Description of the Drawings

5 Figure 1A is a schematic diagram of a metal oxide semiconductor field effect transistor configured to operate as a voltage variable capacitor.

Figure 1B is a graph of a typical MOSFET capacitance versus voltage curve.

10 Figure 1C is a graph of the noise across a MOSFET operating in the depletion mode and coupled to a noisy voltage signal versus the capacitor noise across a MOSFET operating in the inversion mode and coupled to the noisy voltage signal.

Figure 2A is an illustration of one embodiment of an electronic device of the present invention.

15 Figure 2B is an illustration of one embodiment of an electronic device of the present invention configured in a circuit to decouple a high voltage level.

Figure 3 is an illustration of schematic diagram of one embodiment of a circuit of suitable for use in damping resonant oscillations in a power supply grid.

20 Figure 4 is a schematic diagram of one embodiment of a circuit suitable for use in controlling the voltages on a high voltage node and a low voltage node.

Figure 5 is one embodiment of energy source having a unidirectional noise source signal coupled to a load and a device formed on a substrate.

Description of the Invention

25 In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the claims.

Voltage variable capacitors are capable of decreasing noise signals of one polarity and increasing noise signals of the opposite polarity. A metal oxide semiconductor field effect transistor (MOSFET), fabricated and configured in the embodiments described below, is one type of active device that exhibits this property and can be applied to a variety of signal processing applications.

Figure 1A is a schematic diagram of a metal oxide semiconductor field effect transistor configured to operate as a voltage variable capacitor. Figure 1B is a graph of a typical MOSFET capacitance versus voltage curve. As can be seen from the graph, a MOSFET operating in the inversion mode has an approximately constant capacitance for changes in voltage, and a MOSFET operating in the depletion mode has a capacitance that varies with changes in voltage. In some applications, a MOSFET configured as a voltage variable capacitor provides superior noise performance when compared to a fixed value capacitor.

Figure 1C is a graph of the noise in a MOSFET operating in the depletion mode and coupled to a noisy voltage signal versus the noise in a MOSFET operating in the inversion mode and coupled to the noisy voltage signal. The relationship between the depletion mode capacitor noise, $v_{n2}(t)$, for a variable capacitance and the inversion mode capacitor noise, $v_{n1}(t)$, for a constant capacitance is given by:

$$v_{n2}(t) = \frac{aCo}{K} + \sqrt{\left(\frac{aCo}{K}\right)^2 - \frac{2Co}{K} v_{n1}(t)},$$

where K is a proportionality factor relating the capacitance value of the voltage variable capacitance to the applied voltage, a is a scaling factor for scaling the capacitance value C_0 ,

$$v_{o1}(t) = V_{cc} - v_1(t), \text{ and}$$

$$v_{n2}(t) = V_{CC} - v_2(t).$$

$v_1(t)$ is the node voltage of a capacitor being discharged by a constant current and is given by:

$$v_1(t) = V_{CC} - \frac{It}{C_0} .$$

$v_2(t)$ is the node voltage of a variable capacitor being discharged by a constant current.

5 And the capacitance of the voltage variable capacitance as a function of the voltage $v_2(t)$ is given by:

$$c(v_2(t)) = aC_0 - K(V_{CC} - v_2(t)).$$

10 Referring to Figure 1C, data point 103 shows that for an inversion mode capacitor having a noise value of about $\sim .10$, the depletion mode capacitor has a noise value of less than $\sim .10$. So, the MOSFET operating in the depletion mode and having a voltage variable capacitance characteristic is capable of reducing the noise level below the noise level for a MOSFET operating in the inversion mode having a fixed value capacitor.

15 Since equation (1) is a general equation describing the relationship between a noise voltage signal at a node coupled to a fixed value capacitor and a noise voltage signal at a node coupled to a voltage variant capacitor, equation (1) is not limited to MOSFET embodiments.

20 One embodiment of an electronic device having the superior noise performance described above is illustrated in Figure 2A and described below. Figure 2A shows an illustration of one embodiment of a MOSFET fabricated on substrate 203.

25 Substrate 203 includes a pair of spaced apart source and drain regions 206 and 209. Channel region 212 is located between source diffusion region 206 and drain diffusion region 209. Gate oxide layer 215 is formed above channel region 212.

Polysilicon gate layer 218 is formed above gate oxide layer 215.

Substrate 203, which forms the foundation of electronic device 200, is not limited to a particular material. Substrate 203, for one embodiment, is a semiconductor, such as

germanium or silicon. Alternatively, substrate 203 is gallium arsenide, silicon-on-sapphire, or any other crystalline or amorphous material suitable for use as a substrate in the manufacture of electronic devices. For the fabrication of CMOS devices, substrate 203 is preferably n-type silicon.

5 Diffusion regions 206 and 209, for one embodiment, are n+ regions formed in substrate 203. Dopants used in forming source diffusion region 206 and drain diffusion region 209 may be diffused, implanted, or deposited below the surface of substrate 203.

10 Gate oxide layer 215 is formed above channel region 212, and in one embodiment gate oxide layer 215 is thin. A thin gate oxide layer 215 has a thickness of between about 20 and 40 angstroms. A thickness of less than about 20 angstroms may result in manufacturing devices that have low yields, while a thickness of more than about 40 angstroms may result in a device frequency response that is lower than desired. Gate oxide layer 215 is not limited to a particular form of silicon oxide. For one embodiment, gate oxide layer 215 is a thermal oxide, such as silicon oxide (SiO), formed by oxidizing substrate 203. In an alternate embodiment, gate oxide layer 215 is silicon dioxide (SiO₂) thermally grown to the required thickness. Alternatively, gate oxide layer 215 is formed above channel area 212 by chemical vapor deposition (CVD). Forming gate oxide layer 215 by CVD permits gate oxide layer 215 to have a higher doping level than thermally growing gate oxide layer 215.

15 20 Polysilicon gate layer 218, for one embodiment, is an p+ region formed in polysilicon. The dopants for polysilicon gate layer 218 can be diffused, implanted or deposited into the polysilicon gate layer 218. For one embodiment, polysilicon layer 218 has a thickness of about 200 angstroms.

25 In operation, electronic device 200 is configured as shown in Figure 2B. Source diffusion region 206, drain diffusion region 209, and semiconductor substrate 203 are coupled to a low voltage level, such as ground. Gate oxide layer 215 is coupled to high voltage level, V_{GS} 221, such as 1.3 volts. Depletion region 224, shown in Figure 2B, forms a capacitance capable of being discharged at a constant rate. For the depletion region capacitance being discharged at a constant rate, the gate-to-drain voltage is given by:

$$v_2(t) = V_{cc} - \frac{aCo}{K} - \sqrt{\left(\frac{aCo}{K}\right)^2 - \frac{2It}{K}}.$$

The gate-to-drain voltage, $v_2(t)$, is a non-linear function of time.

5 Electronic device 200 shown in Figure 2A is suitable for use in a variety of signal processing applications. However, devices configured as voltage variable capacitors and fabricated on an integrated circuit substrate are especially useful in damping resonant oscillations in voltage supply grid networks. Resonant oscillations are common in voltage supply grid networks included in synchronous digital systems, such as microprocessors.

10 A microprocessor power supply grid network can be driven into resonant oscillations by large transient current events, which occur during the normal synchronous operation of the microprocessor. Microprocessors are fabricated on a die and the frequency of the resonant oscillations is dependent on the inductance value between the power source and the die and the total capacitance seen on the die by the power supply grid network. Since high frequencies tend to die away quickly, faster damping of the power supply resonant behavior is obtained by transforming the power supply resonant spectrum to higher frequencies. One method of transforming the resonant spectrum to higher frequencies is to add voltage variable capacitors to the power supply grid network. Voltage variable capacitors are capable of decreasing noise of one polarity and increasing noise of the opposite polarity in response to a changing voltage. If the voltage variable capacitors are added to decrease noise when the voltage tends to decrease and to amplify noise when the voltage tends to increase, the frequency content of the power supply resonance is changed and the voltage stability of the power supply grid network is improved.

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network*

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Figure 3 is an illustration of a power supply grid network coupled to logic cells 303 located on an integrated circuit, such as flip-chip 304. The power supply grid network includes power supply voltage nodes 305, logic cells 303, and fixed decoupling capacitors 306. Each of the flip-chip logic cells 303 is decoupled by a number of fixed capacitors 306. For one embodiment, each of the number of fixed capacitors 306 has a capacitance value of about 100 femto-farads. The number of fixed capacitors is selected to provide a capacitance sufficient to avoid a significant voltage droop in voltage at power supply nodes 305 during the normal operation of logic cells 303. For one embodiment, the capacitance value of each of the variable capacitors 309 is about one-hundred nano-farads. The number of variable capacitors added to the power supply grid is selected based on the characteristics of the resonant voltages, which may be determined through simulation of the power supply grid network and through experiments performed on the power supply grid network coupled to flip chip 305.

Processors, such as microprocessors, have core circuits fabricated at smaller dimensions and these core circuits typically operate off a lower voltage than non-core circuits. Figure 4 is a schematic diagram of one embodiment of a circuit suitable for use in controlling the voltages on high voltage node 403 and low voltage node 406 provided by an energy sources 407 and 408 in a microprocessor power distribution circuit. For one embodiment, low voltage node 406 is coupled to 1 volt and high voltage node 403 is coupled to 1.8 volts. The plurality of voltage variable capacitors 409 connected between the high voltage node 403 and the low voltage node 406 prevents the low voltage node from falling below 1 volt. The plurality of voltage variable capacitors 409 also decreases noise in the direction that tends to increase the voltage on high voltage node 403. For one embodiment, the plurality of voltage variable capacitors are formed in MOSFETs coupled between high voltage node 403 and low voltage node 406. The source, drain, and body of each MOSFET are connected to high voltage node 403, and the gate of each MOSFET is connected to low voltage node 406.

In an alternate embodiment, devices configured as voltage variable capacitors and fabricated on an integrated circuit substrate are useful in suppressing noise in a noise source having a unidirectional noise signal. Figure 5 is one embodiment of energy source

503 having a unidirectional noise source signal coupled to load 506 and device 509 formed on substrate 512. For one embodiment, device 509 is a MOSFET configured as a variable voltage capacitor. For this embodiment, device 509 is capable of suppressing the unidirectional noise source signal more than a fixed voltage variable capacitor. This capability permits load 506 to be designed having lower noise margins and a lower operating voltage. Designing load 506 for operation at a lower operating voltage allows load 506 to operate longer on a depletable energy source, such as a battery.

10 Although specific embodiments have been illustrated and described herein, it will be appreciated by those of skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.